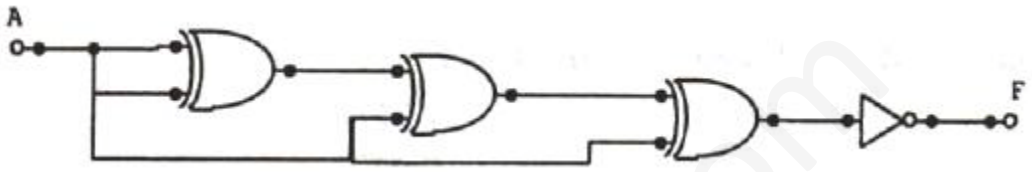
BCA101 - Digital Electronics

Multiple Choice Questions

1. i) The maximum positive number that can be represented in 1's complement representation is

   a) $2^{n-1} - 1$
   b) $1 - 2^{n-1}$
   c) $-(2^{n-1} - 1)$
   d) 2^{n-1}

   ii) The value of F is



   a) 0
   b) 1
   c) A
   d) A'

   iii) A decoder with enable input can be used as

   a) Encoder
   b) Parity Generator
   c) NAND
   d) Demultiplexer

   iV) Which of the following is self-complementing code?

   a) Gray
   b) Excess-3
   c) BCD
   d) Parity code
   e) Hamming code

   v) How many Flip-flops are required to design MOD-1024 counter?

   a) 1024
   b) 102
   c) 10
   d) 1

   vi) The decimal equivalent of the binary number $(101111.1101)_2$ is

   a) $(46.8125)_{10}$
   b) $(47.8125)_{10}$
   c) $(47.8155)_{10}$
   d) $(47.8145)_{10}$

   vii) Which family has the better noise margin?

   a) ECL
   c) DTL

b) MOS
d) TTL

viii) J-K flip – flop has

a) one stable state
b) two stable state
c) no stable state
d) none of these

ix) Master-slave configuration is used in flip-flops to

a) increase its clicking rate
b) reduce power dissipation
c) eliminate race around condition
d) improve its reliability

x) The equation $\sqrt{213} = 13$ is valid for which one of the number syatems with base?

a) Base 8
c) Base 6

b) Base 6
d) Base 4

xi) Simplified form of Boolean expression

F (A, B, C) = ABC + A'BC + AB'C + ABC' is

a) AB + BC + CA
b) A + BC + CA
c) AB + B + CA
d) ABC + A + B + C

xii) PROMs are used primarily for

a) data storage
b) temporary program and data storage
c) they are inexpensive
d) permanent program & data storage

Short Answer Type Questions

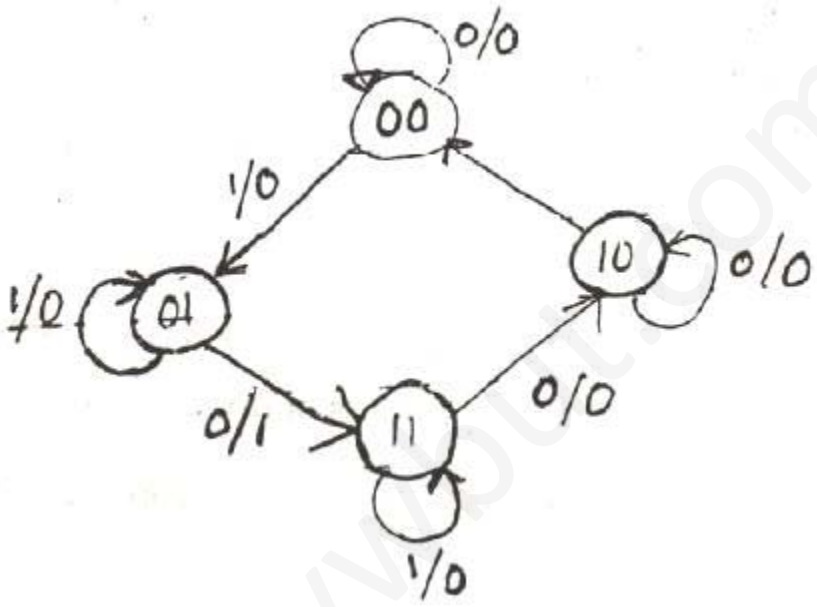
2. Implement a full adder circuit using decoder.
3. Design a combinational circuit using an 8 x 4 ROM that accepts a 3-bit number & generates an output binary number equal to the square of input no.
4. Simplify the following expression using K-map
   Y = π (0, 1, 4, 5, 6, 8, 9, 12, 13, 14)
5. Check whether the Even parity Hamming code for 4-bit data, $(1001011)_2$ is correct or not. If not, correct the code.
6. Explain race around condition of J-K flip-flop. Show how this condition can be avoided.
7. Perform the arithmetic operation:

$(-22)_{decimal} + (13)_{decimal} + (-15)_{decimal}$

Using 2's complement binary form.

Long Answer Type Questions

8. a) Design an asynchronous 4-bit up-down counter and it will count up when a signal line M = 0 and count down when a signal line M = 1.
   b) Design a sequential circuit that implements the following state diagram. Use all D-type FF for the design.



9. a) Write down the excitation table of JK and D flip-flops. Derive the excitation equations for theses two flip-flops.
   b) Design a clocked R-S flip-flop using NAND gates. Explain its principle of operation.

10. a) Simplify the following function using K-map.
    i) $F = \pi m (0, 1, 3, 8, 10, 15) . \pi d (11, 13, 14)$
    ii) $F = \Sigma m (0, 4, 7, 9, 13, 15) + \Sigma d (10, 14)$

    b) What is ROM and RAM? What is the basic difference between EPROM and EEROM?

11. a) Draw a neat diagram for a R-2R ladder type DAC. What is linearity error and offset error in a DAC?
    c) Find the conversion time of a successive approximation A/D converter which uses a 2 MHz clock and a 5-bit binary ladder containing 8V reference. What is the conversion rate?

12. Write short notes on any three of the following:
    a) CMOS Logic
    b) Tri-state gates in TTL family
    c) A/D convertor
    d) Data lock-out in a counter
    e) EPROM