Operational Amplifiers:

The operational amplifier is a direct-coupled high gain amplifier usable from 0 to over 1MH Z to which feedback is added to control its overall response characteristic i.e. gain and bandwidth. The op-amp exhibits the gain down to zero frequency.

Such direct coupled (dc) amplifiers do not use blocking (coupling and by pass) capacitors since these would reduce the amplification to zero at zero frequency. Large by pass capacitors may be used but it is not possible to fabricate large capacitors on a IC chip. The capacitors fabricated are usually less than 20 pf. Transistor, diodes and resistors are also fabricated on the same chip.

Differential Amplifiers:

Differential amplifier is a basic building block of an op-amp. The function of a differential amplifier is to amplify the difference between two input signals.

How the differential amplifier is developed? Let us consider two emitter-biased circuits as shown in **fig. 1**.

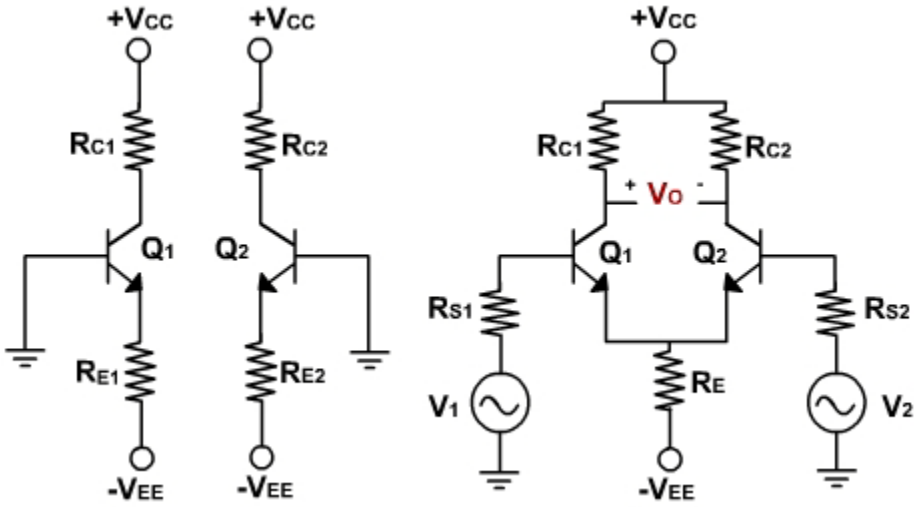


Fig. 1

The two transistors Q_1 and Q_2 have identical characteristics. The resistances of the circuits are equal, i.e. $R_{E1} = R_{E2}$, $R_{C1} = R_{C2}$ and the magnitude of $+V_{CC}$ is equal to the magnitude of $-V_{EE}$. These voltages are measured with respect to ground.

To make a differential amplifier, the two circuits are connected as shown in **fig. 1**. The two $+V_{CC}$ and $-V_{EE}$ supply terminals are made common because they are same. The two emitters are also connected and the parallel combination of R_{E1} and R_{E2} is replaced by a resistance R_E. The two input signals v_1 & v_2 are applied at the base of Q_1 and at the base of Q_2. The output voltage is

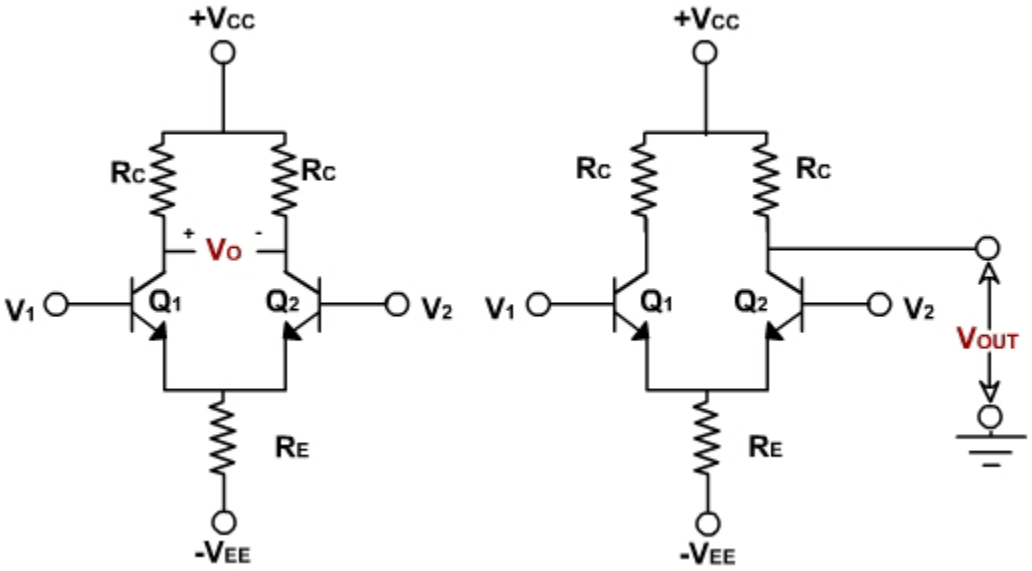
taken between two collectors. The collector resistances are equal and therefore denoted by R_C = R_{C1} = R_{C2}.

Ideally, the output voltage is zero when the two inputs are equal. When v_1 is greater then v_2 the output voltage with the polarity shown appears. When v_1 is less than v_2, the output voltage has the opposite polarity.

The differential amplifiers are of different configurations.

The four differential amplifier configurations are following:

1. Dual input, balanced output differential amplifier.
2. Dual input, unbalanced output differential amplifier.
3. Single input balanced output differential amplifier.
4. Single input unbalanced output differential amplifier.



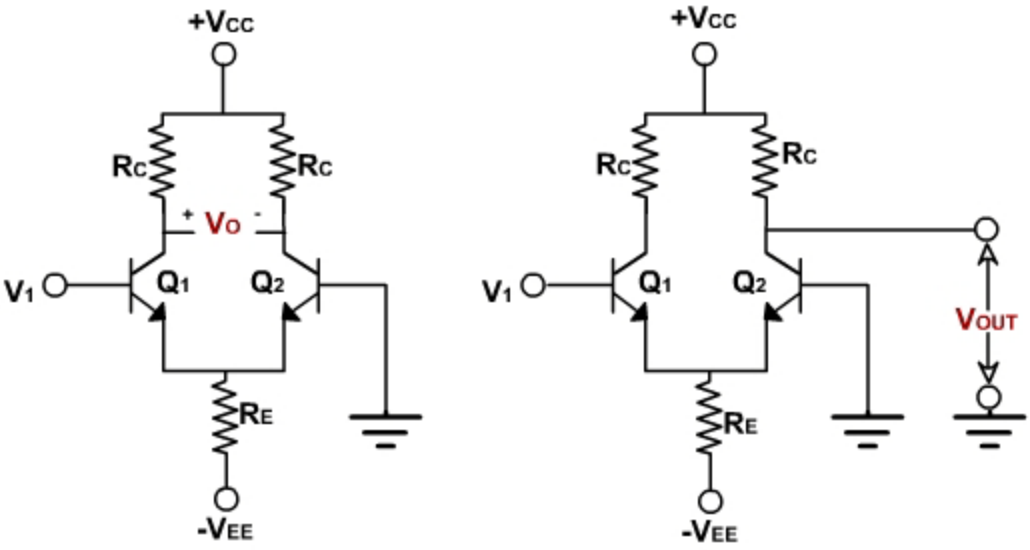


Fig. 2

These configurations are shown in **fig. 2**, and are defined by number of input signals used and the way an output voltage is measured. If use two input signals, the configuration is said to be dual input, otherwise it is a single input configuration. On the other hand, if the output voltage is measured between two collectors, it is referred to as a balanced output because both the collectors are at the same dc potential w.r.t. ground. If the output is measured at one of the collectors w.r.t. ground, the configuration is called an unbalanced output.

A multistage amplifier with a desired gain can be obtained using direct connection between successive stages of differential amplifiers. The advantage of direct coupling is that it removes the lower cut off frequency imposed by the coupling capacitors, and they are therefore, capable of amplifying dc as well as ac input signals.

Dual Input, Balanced Output Differential Amplifier:

The circuit is shown in **fig. 1,** v_1 and v_2 are the two inputs, applied to the bases of Q_1 and Q_2 transistors. The output voltage is measured between the two collectors C_1 and C_2 , which are at same dc potentials.

D.C. Analysis:

To obtain the operating point (I_{CC} and V_{CEQ}) for differential amplifier dc equivalent circuit is drawn by reducing the input voltages v_1 and v_2 to zero as shown in **fig. 3**.

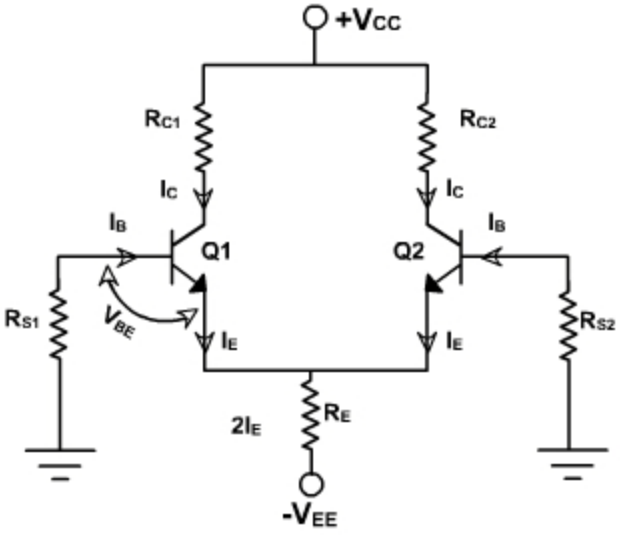


Fig. 3

The internal resistances of the input signals are denoted by R_S because $R_{S1}= R_{S2}$. Since both emitters biased sections of the different amplifier are symmetrical in all respects, therefore, the operating point for only one section need to be determined. The same values of I_{CQ} and V_{CEQ} can be used for second transistor Q_2.

Applying KVL to the base emitter loop of the transistor Q_1.

$$R_S I_B + V_{BE} + 2 I_E R_E = V_{EE}$$

But $I_B = \frac{I_E}{\beta_{dc}}$ and $I_C \approx I_E$

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E + R_S / \beta_{dc}} \qquad (E\text{-}1)$$

$V_{BE} = 0.6V$ for S_i and $0.2V$ for G_e.

Generally $\frac{R_S}{\beta_{dc}} << 2R_E$ because R_S is the internal resistance of input signal.

$$\therefore I_E = I_C = \frac{V_{EE} - V_{BE}}{2R_E}$$

The value of R_E sets up the emitter current in transistors Q_1 and Q_2 for a given value of V_{EE}. The emitter current in Q_1 and Q_2 are independent of collector resistance R_C.

The voltage at the emitter of Q_1 is approximately equal to $-V_{BE}$ if the voltage drop across R is negligible. Knowing the value of I_C the voltage at the collector $V_C$is given by

$$V_C = V_{CC} - I_C R_C$$

and $V_{CE} = V_C - V_E$

$= V_{CC} - I_C R_C + V_{BE}$

$V_{CE} = V_{CC} + V_{BE} - I_C R_C$ (E-2)

From the two equations V_{CEQ} and I_{CQ} can be determined. This dc analysis applicable for all types of differential amplifier.

Example - 1

The following specifications are given for the dual input, balanced-output differential amplifier of **fig.1:**
$R_C = 2.2\ k\Omega$, $R_B = 4.7\ k\Omega$, $R_{in\,1} = R_{in\,2} = 50\ \Omega$, $+V_{CC} = 10V$, $-V_{EE} = -10\ V$, $\beta_{dc} = 100$ and $V_{BE} = 0.715V$.
Determine the operating points (I_{CQ} and V_{CEQ}) of the two transistors.

Solution:

The value of I_{CQ} can be obtained from equation (E-1).

$$I_{CQ} = I_E = \frac{V_{EE} - V_{BE}}{2R_E + R_{in}/\beta_{dc}}$$

$$= \frac{10 - 0.715}{9.4k\Omega + 50/100} = 0.988mA$$

The voltage V_{CEQ} can be obtained from equation (E-2).

$$V_{CEQ} = V_{CC} + V_{BB} - R_C I_{CQ}$$
$$= 10 + 0.715 - (2.2k\Omega)(0.988mA)$$
$$= 8.54V$$

The values of I_{CQ} and V_{CEQ} are same for both the transistors.

Dual Input, Balanced Output Difference Amplifier:

The circuit is shown in **fig. 1** v_1 and v_2 are the two inputs, applied to the bases of Q_1 and Q_2 transistors. The output voltage is measured between the two collectors C_1 and C_2, which are at same dc potentials.

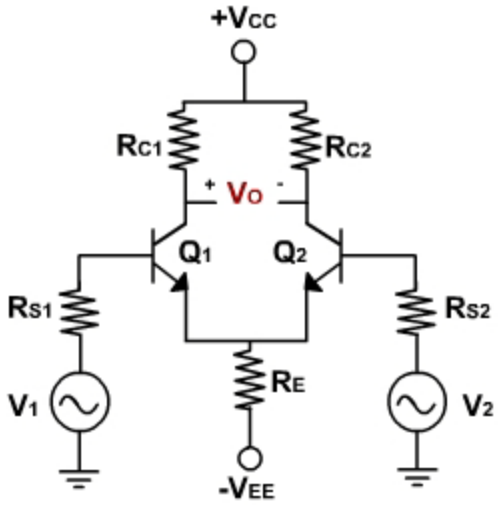


Fig. 1

A.C. Analysis :

In previous lecture dc analysis has been done to obtain the operatiing point of the two transistors.

To find the voltage gain A_d and the input resistance R_i of the differential amplifier, the ac equivalent circuit is drawn using r-parameters as shown in **fig. 2**. The dc voltages are reduced to zero and the ac equivalent of CE configuration is used.

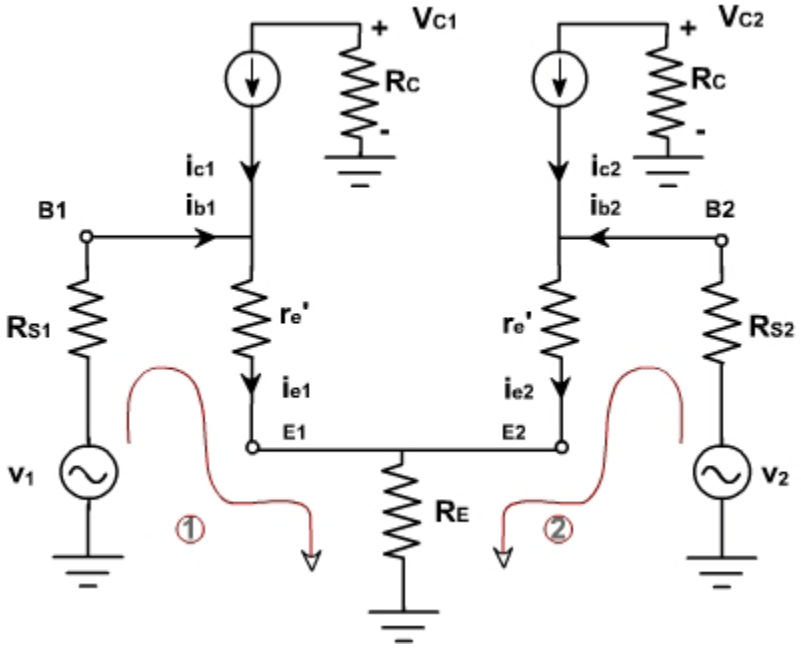


Fig. 2

Since the two dc emitter currents are equal. Therefore, resistance r'_{e1} and r'_{e2} are also equal and designated by r'_e . This voltage across each collector resistance is shown 180° out of phase with respect to the input voltages v_1 and v_2. This is same as in CE configuration. The polarity of the output voltage is shown in Figure. The collector C_2 is assumed to be more positive with respect to collector C_1 even though both are negative with respect to to ground.

Applying KVL in two loops 1 & 2.

$$v_1 = R_{S1}\, i_{b1} + i_{e1}\, r'_e + (i_{e1} + i_{e2})\, R_E$$
$$v_2 = R_{S2}\, i_{b2} + i_{e2}\, r'_e + (i_{e1} + i_{e2})\, R_E$$

Substituting current relations,

$$i_{b1} = \frac{i_{e1}}{\beta},\quad i_{b2} = \frac{i_{e2}}{\beta}$$
$$V_1 = \frac{R_{S1}}{\beta}\, i_{e1} + r'_e\, i_{e1} + R_E\, (i_{e1} + i_{e2})$$
$$V_2 = \frac{R_{S2}}{\beta}\, i_{e2} + r'_e\, i_{e2} + R_E\, (i_{e1} + i_{e2})$$

Again, assuming R_{S1} / b and R_{S2} / b are very small in comparison with R_E and r_e' and therefore neglecting these terms,

$$(r'_e + R_E)\, i_{e1} + R_E\, i_{e2} = v_1$$
$$R_E\, i_{e1} + (r'_e + R_E)\, i_{e2} = v_2$$

Solving these two equations, i_{e1} and i_{e2} can be calculated.

$$i_{e1} = \frac{(r'_e + R_E)\, v_1 - R_E\, v_2}{(r'_e + R_E)^2 - R_E^2}$$
$$i_{e2} = \frac{(r'_e + R_E)\, v_2 - R_E\, v_1}{(r'_e + R_E)^2 - R_E^2}$$

The output voltage V_O is given by

$V_O = V_{C2} - V_{C1}$

$= -R_C\, i_{C2} - (-R_C\, i_{C1})$

$= R_C\, (i_{C1} - i_{C2})$

$= R_C\, (i_{e1} - i_{e2})$

Substituting i_{e1}, & i_{e2} in the above expression

$$v_o = R_C\left\{\frac{(r_e + R_E)V_1 - R_E V_2}{(r'_e + R_E)^2 - R_E^2} - \frac{(r_e + R_E)V_2 - R_E V_1}{(r'_e + R_E)^2 - R_E^2}\right\}$$

$$= \frac{R_C(v_1 - v_2)(r'_e - 2R_E)}{r'_e(r'_e + 2R_E)}$$

$$\text{Therefore}, v_o = \frac{R_C}{r'_e}(v_1 - v_2) \qquad \text{(E-1)}$$

Thus a differential amplifier amplifies the difference between two input signals. Defining the difference of input signals as $v_d = v_1 - v_2$ the voltage gain of the dual input balanced output differential amplifier can be given by

$$A_d = \frac{v_C}{v_d} = \frac{R_C}{r'_e} \qquad \text{(E-2)}$$

Differential Input Resistance:

Differential input resistance is defined as the equivalent resistance that would be measured at either input terminal with the other terminal grounded. This means that the input resistance R_{i1} seen from the input signal source v_1 is determined with the signal source v_2 set at zero. Similarly, the input signal v_1 is set at zero to determine the input resistance R_{i2} seen from the input signal source v_2. Resistance R_{S1} and R_{S2} are ignored because they are very small.

$$R_{i1} = \left.\frac{v_1}{i_{b1}}\right|_{v_2 = 0}$$

$$= \left.\frac{v_1}{i_{e1}/\beta}\right|_{v_2 = 0}$$

Substituting i_{e1},

$$R_{i1} = \frac{\beta r'_e(r'_e + 2R_E)}{r'_e + R_E}$$

$$\text{Since } R_E >> r'_e$$

$$\therefore \quad r'_e + 2R_E >> 2R_E$$

$$\text{or} \quad r'_e + R_E >> R_E$$

$$\therefore R_{i1} = 2\beta r_e' \qquad \text{(E-3)}$$

Similarly,

$$R_{i2} = \left.\frac{V_2}{i_{b2}}\right|_{V_1=0}$$

$$= \left.\frac{V_2}{i_{e2}/\beta}\right|_{V_1=0}$$

$$R_{i2} = 2\beta r'_e \qquad (E-4)$$

The factor of 2 arises because the r_e' of each transistor is in series.

To get very high input impedance with differential amplifier is to use Darlington transistors. Another ways is to use FET.

Output Resistance:

Output resistance is defined as the equivalent resistance that would be measured at output terminal with respect to ground. Therefore, the output resistance R_{O1} measured between collector C_1 and ground is equal to that of the collector resistance R_C. Similarly the output resistance R_{O2} measured at C_2 with respect to ground is equal to that of the collector resistor R_C.

$R_{O1} = R_{O2} = R_C$ (E-5)

The current gain of the differential amplifier is undefined. Like CE amplifier the differential amplifier is a small signal amplifier. It is generally used as a voltage amplifier and not as current or power amplifier.

Example - 1

The following specifications are given for the dual input, balanced-output differential amplifier: R_C = 2.2 kΩ, R_B = 4.7 kΩ, $R_{in\,1} = R_{in\,2}$ = 50Ω, $+V_{CC}$= 10V, $-V_{EE}$ = -10 V, β_{dc} =100 and V_{BE} = 0.715V.

a. Determine the voltage gain.
b. Determine the input resistance
c. Determine the output resistance.

Solution:

(a). The parameters of the amplifiers are same as discussed in example-1 of lecture-1. The operating point of the two transistors obtained in lecture-1 are given below

I_{CQ} = 0.988 mA
V_{CEQ}=8.54V

The ac emitter resistance

$$r_e' = \frac{25mV}{I_E mA} = \frac{25mV}{0.988mA} = 25.3\Omega$$

Therefore, substituting the known values in voltage gain equation (E-2), we obtain

$$A_d = \frac{v_o}{v_{id}} = \frac{R_C}{r_e} = \frac{2.2\,k\Omega}{25.3} = 86.96$$

b). The input resistance seen from each input source is given by (E-3) and (E-4):

$$R_{i1} = R_{i2} = 2\beta_{ac} r_e = (2)(100)(25.3) = 5.06k\Omega$$

(c) The output resistance seen looking back into the circuit from each of the two output terminals is given by (E-5)

$R_{o1} = R_{o2} = 2.2\ k\ \Omega$

Example - 2

For the dual input, balanced output differential amplifier of Example-1:

a. Determine the output voltage (v_o) if $v_{in\,1}$ = 50mV peak to peak (pp) at 1 kHz and $v_{in\,2}$ = 20 mV pp at 1 kHz.
b. What is the maximum peal to peak output voltage without clipping?

Solution:

(a) In Example-1 we have determined the voltage gain of the dual input, balanced output differential amplifier. Substituting this voltage gain (A_d = 86.96) and given values of input voltages in (E-1), we get

$$v_o = \frac{R_C}{r_e}(v_{in1} - v_{in2}) = 86.96\,(50mv - 20mV)$$
$$= 2.61\ Vpp$$

(b) Note that in case of dual input, balanced output difference amplifier, the output voltage v_o is measured across the collector. Therefore, to calculate the maximum peak to peak output voltage, we need to determine the voltage drop across each collector resistor:

$$V_{R_C} = R_C I_C$$

Substituting $I_C = I_{CQ}$ = 0.988 mA, we get

$$V_{R_C} = (2.2k\Omega)(0.988mA) = 2.17V < V_{CE} = 8.54V$$

This means that the maximum change in voltage across each collector resistor is ± 2.17 (ideally) or 4.34 V_{PP}. In other words, the maximum peak to peak output voltage with out clipping is (2) (4.34) = 8.68 V_{PP}.

A dual input, balanced output difference amplifier circuit is shown in **fig. 1**.

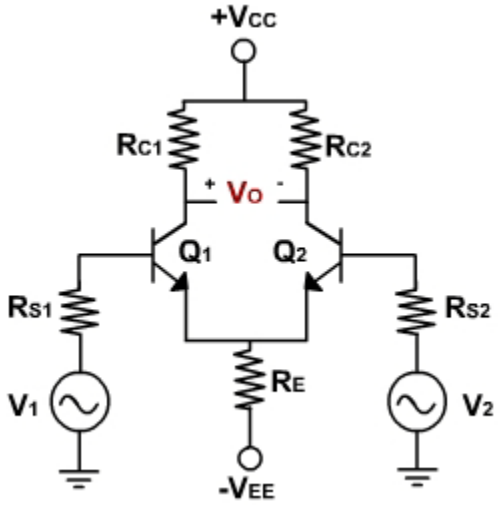


Fig. 1

Inverting & Non – inverting Inputs:

In differential amplifier the output voltage v_O is given by

$$V_O = A_d (v_1 - v_2)$$

When $v_2 = 0$, $v_O = A_d v_1$
& when $v_1 = 0$, $v_O = - A_d v_2$

Therefore the input voltage v_1 is called the non inventing input because a positive voltage v_1 acting alone produces a positive output voltage v_O. Similarly, the positive voltage v_2 acting alone produces a negative output voltage hence v_2 is called inverting input. Consequently B_1 is called noninverting input terminal and B_2 is called inverting input terminal.

Common mode Gain:

A common mode signal is one that drives both inputs of a differential amplifier equally. The common mode signal is interference, static and other kinds of undesirable pickup etc.

The connecting wires on the input bases act like small antennas. If a differential amplifier is operating in an environment with lot of electromagnetic interference, each base picks up an

unwanted interference voltage. If both the transistors were matched in all respects then the balanced output would be theoretically zero. This is the important characteristic of a differential amplifier. It discriminates against common mode input signals. In other words, it refuses to amplify the common mode signals.

The practical effectiveness of rejecting the common signal depends on the degree of matching between the two CE stages forming the differential amplifier. In other words, more closely are the currents in the input transistors, the better is the common mode signal rejection e.g. If v_1 and v_2 are the two input signals, then the output of a practical op-amp cannot be described by simply

$v_0 = A_d (v_1 \text{ } v_2)$

In practical differential amplifier, the output depends not only on difference signal but also upon the common mode signal (average).

$v_d = (v_1 \text{ } v_d)$

and $v_C = ½ (v_1 + v_2)$

The output voltage, therefore can be expressed as

$v_O = A_1 v_1 + A_2 v_2$

Where A_1 & A_2 are the voltage amplification from input 1(2) to output under the condition that input 2 (1) is grounded.

$$\therefore v_1 = v_C + \frac{1}{2}v_d \quad , \quad v_2 = v_C - \frac{1}{2}v_d$$

Substituting V_1 & V_2 in output voltage equation

$$v_O = A_1 \left(v_C + \frac{1}{2}v_d\right) + A_2 \left(v_C - \frac{1}{2}v_d\right)$$

$$= \frac{1}{2}(A_1 - A_2)\, v_d + (A_1 - A_2)\, v_C$$

$$= A_d v_d + A_C v_C$$

The voltage gain for the difference signal is A_d and for the common mode signal is A_C.

The ability of a differential amplifier to reject a common mode signal is expressed by its common mode rejection ratio (CMRR). It is the ratio of differential gain A_d to the common mode gain A_C.

$$\text{CMRR} = \frac{A_d}{A_C} = \rho$$

$$\therefore v_O = A_d V_d \left(1 + \frac{1}{\rho}\frac{V_C}{V_d}\right)$$

Date sheet always specify CMRR in decibels CMRR = 20 log CMRR.

Therefore, the differential amplifier should be designed so that r is large compared with the ratio of the common mode signal to the difference signal. If r = 1000, v_C = 1mV, v_d = 1 m V, then

$$\frac{1}{\rho}\frac{V_C}{V_d} = \frac{1}{1000} \times \frac{1000\,\mu V}{1\,\mu V} = 1$$

It is equal to first term. Hence for an amplifier with r = 1000, a 1m V difference of potential between two inputs gives the same output as 1mV signal applied with the same polarity to both inputs.

Dual Input, Unbalanced Output Differential Amplifier:

In this case, two input signals are given however the output is measured at only one of the two-collector w.r.t. ground as shown in **fig. 2**. The output is referred to as an unbalanced output because the collector at which the output voltage is measured is at some finite dc potential with respect to ground..

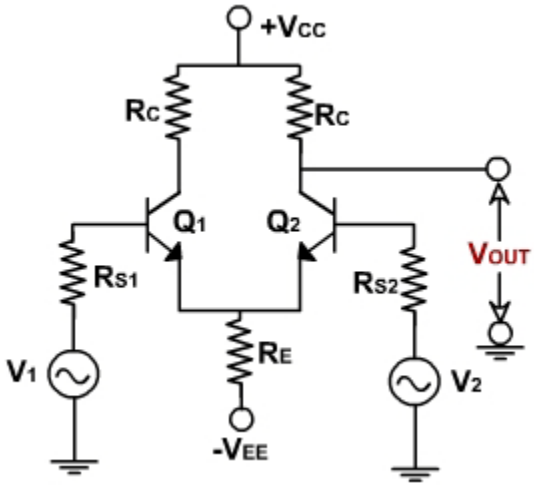


Fig. 2

In other words, there is some dc voltage at the output terminal without any input signal applied. DC analysis is exactly same as that of first case.

$$I_E = I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + R_2/\beta_{dc}}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ}R_C$$

AC Analysis:

The output voltage gain in this case is given by

$$A_d = \frac{V_0}{V_d} = \frac{R_C}{2r'_e}$$

The voltage gain is half the gain of the dual input, balanced output differential amplifier. Since at the output there is a dc error voltage, therefore, to reduce the voltage to zero, this configuration is normally followed by a level translator circuit.

Differential amplifier with swamping resistors:

By using external resistors R'_E in series with each emitter, the dependence of voltage gain on variations of r'_e can be reduced. It also increases the linearity range of the differential amplifier.

Fig. 3, shows the differential amplifier with swamping resistor R'_E. The value of R'_E is usually large enough to swamp the effect of r'_e.

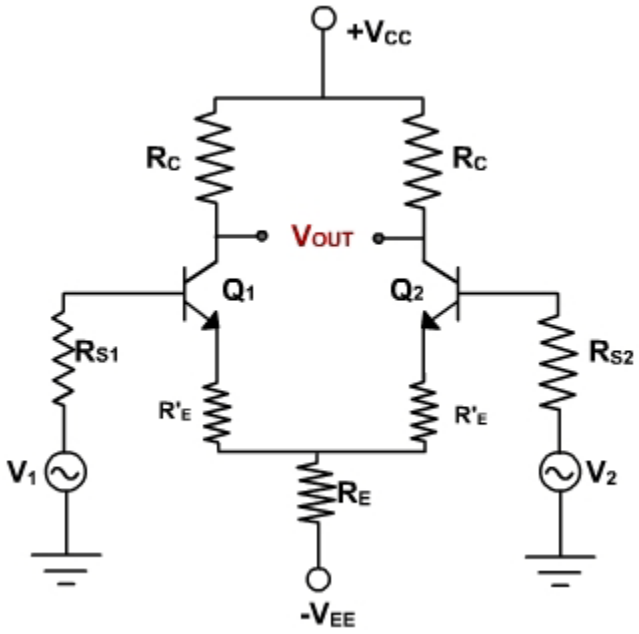


Fig. 3

$$R_1 I_B + V_{BE} + R'_E I_E + 2 R_E I_E = V_{EE}$$

$$R_1 I_E / \beta_{dc} + V_{BE} + R'_E I_E + 2 R_E I_E = V_{EE}$$

From the equation, I_E can be obtained as

$$I_E = \frac{V_{EE} - V_{BE}}{R'_E + 2R_E + R_1 / \beta_{dc}}$$

$$V_{CEQ} = V_{CC} + V_{BE} - I_{CQ} R_C$$

The new voltage gain is given by $A_d = \frac{R_C}{r_e + R_E}$

The input resistance is given by $R_{i1} = R_{i2} = 2\beta (r'_e + R'_E)$

The output resistance with or without R'_E is the same i.e.

$$R_{01} = R_{01} = R_C$$

Example-1

Consider example-1 of lecture-2. The specifications are given again for the dual input, unbalanced-output differential amplifier: R_C = 2.2 kΩ, R_B= 4.7 kΩ, $R_{in1} = R_{in2}$= 50Ω, $+V_{CC}$ = 10V, $-V_{EE}$= -10 V, β_{dc} =100 and V_{BE}= 0.715V.

Determine the voltage gain, input resistance and the output resistance.

Solution:

Since the component values remain unchanged and the biasing arrangement is same, the I_{CQ} and V_{CEQ} values as well as input and output resistance values for the dual input, unbalanced output configuration must be the same as those for the dual input, balanced output configuration.

Thus, I_{CQ} = 0.988 mA
V_{CEQ} = 8.54 V
$R_{i1} = R_{i2}$ = 5.06 kΩ
R_o = 2.2 kΩ

The voltage gain of the dual input, unbalanced output differential amplifier is given by

$$A_d = \frac{R_C}{2r_e} = \frac{2.2\ k\Omega}{(2)(25.3)} = 43.8$$

Example-2

Repeat Example-1 for single input, balanced output differential amplifier.

Solution:

Because the same biasing arrangement and same component values are used in both configurations, the results obtained in Example-1 for the dual input, balanced output configuration are also valid for the single input, balanced output configuration.

That is,

I_{CQ}= 0.988 mA
V_{CEQ} = 8.54 V
V_d = 86.96
R_i = 5.06 kΩ
R_{o1} = R_{o2} = 2.2 kΩ

Biasing of Differential Amplifiers

Constant Current Bias:

In the dc analysis of differential amplifier, we have seen that the emitter current I_E depends upon the value of b_{dc}. To make operating point stable I_E current should be constant irrespective value of b_{dc}.

For constant I_E, R_E should be very large. This also increases the value of CMRR but if R_E value is increased to very large value, I_E (quiescent operating current) decreases. To maintain same value of I_E, the emitter supply V_{EE} must be increased. To get very high value of resistance R_E and constant I_E, current, current bias is used.

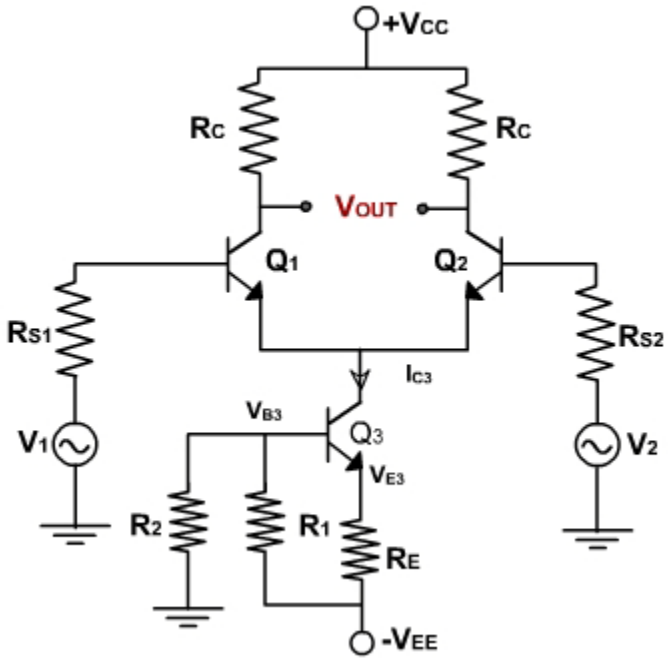


Figure 5.1

Fig. 1, shows the dual input balanced output differential amplifier using a constant current bias. The resistance R_E is replace by constant current transistor Q_3. The dc collector current in Q_3 is established by R_1, R_2, & R_E.

Applying the voltage divider rule, the voltage at the base of Q_3 is

$$V_{B3} = \frac{R_2}{R_1+R_2}(-V_{EE})$$

$$V_{E3} = V_{B3} - V_{BE3}$$

$$= -\frac{R_2}{R_1+R_2} V_{EE} - V_{BE3}$$

$$I_{BE3} = I_{C3} = \frac{V_{E3}-(-V_{EE})}{R_E}$$

$$= \frac{V_{EE} - \left(\frac{R_2}{R_1+R_2}\right) V_{EE} - V_{BE3}}{R_E}$$

Because the two halves of the differential amplifiers are symmetrical, each has half of the current I_{C3}.

$$I_{E1} = I_{E2} = \frac{I_{C3}}{2} = \frac{V_{EE} - \left[\frac{R_2}{R_1+R_2} V_{EE}\right] - V_{BE3}}{2R_E}$$

The collector current, I_{C3} in transistor Q_3 is fixed because no signal is injected into either the emitter or the base of Q_3.

Besides supplying constant emitter current, the constant current bias also provides a very high source resistance since the ac equivalent or the dc source is ideally an open circuit. Therefore, all the performance equations obtained for differential amplifier using emitter bias are also valid.

As seen in I_E expressions, the current depends upon V_{BE3}. If temperature changes, V_{BE} changes and current I_E also changes. To improve thermal stability, a diode is placed in series with resistance R_1as shown in **fig. 2**.

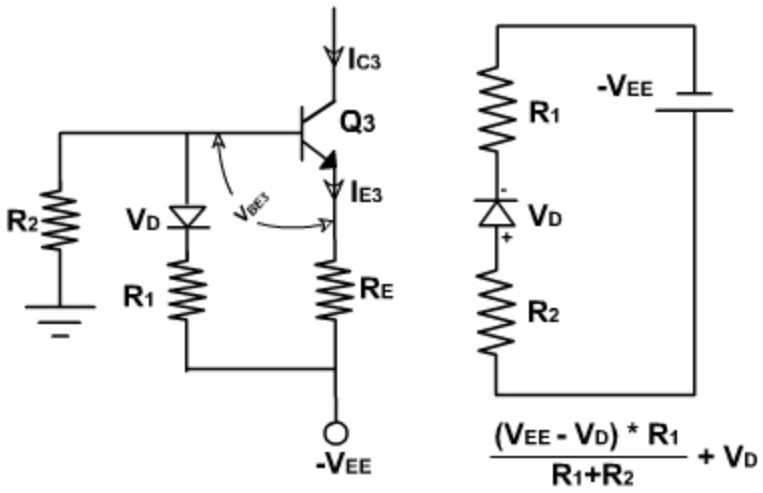


Fig. 2

This helps to hold the current I_{E3} constant even though the temperature changes. Applying KVL to the base circuit of Q_3.

$$(V_{EE} - V_D)\ \frac{R_1}{R_1+R_2} + V_D = V_{BE3} + I_{E3}R_E$$

where V_D is the diode voltage. Thus,

$$I_{E3} = \frac{1}{R_E}\left\{ V_{EE}\ \frac{R_1}{R_1+R_2} + V_D\ \frac{R_1}{R_1+R_2} - V_{BE3} \right\}$$

If R_1 and R_2 are so chosen that

$$\frac{R_2}{R_1+R_2}\ V_D = V_{BE3}$$

then,

$$I_{E3} = \frac{1}{R_3} \cdot \frac{V_{EE}R_1}{R_1+R_2}$$

Therefore, the current I_{E3} is constant and independent of temperature because of the added diode D. Without D the current would vary with temperature because V_{BE3} decreases approximately by 2mV/° C. The diode has same temperature dependence and hence the two variations cancel each other and I_{E3} does not vary appreciably with temperature. Since the cut in voltage V_D of diode approximately the same value as the base to emitter voltage V_{BE3} of a transistor the above condition cannot be satisfied with one diode. Hence two diodes are used in series for V_D. In this case the common mode gain reduces to zero.

Some times zener diode may be used in place of diodes and resistance as shown in **fig. 3**. Zeners are available over a wide range of voltages and can have matching temperature coefficient

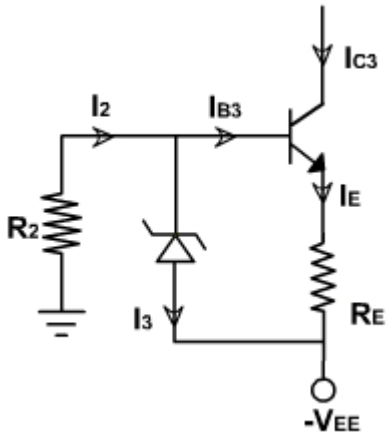


Fig. 3

The voltage at the base of transistor Q_B is

$$V_{B3} = V_Z - V_{EE}$$
$$V_{E3} = V_{B3} - V_{BE3}$$
$$= V_Z - V_{EE} - V_{BE3}$$
$$\therefore I_{E3} = \frac{V_{E3} - (-V_{EE})}{R_E}$$
$$= \frac{V_Z - V_{BE3}}{R_E}$$

The value of R_2 is selected so that $I_2 \gg 1.2\, I_{Z(min)}$ where I_Z is the minimum current required to cause the zener diode to conduct in the reverse region, that is to block the rated voltage V_Z.

$$R_2 = \frac{V_{EE} - V_Z}{I_2}$$
Where $I_2 = 1.2\, I_{Z(min)}$

Current Mirror:

The circuit in which the output current is forced to equal the input current is said to be a current mirror circuit. Thus in a current mirror circuit, the output current is a mirror image of the input current. The current mirror circuit is shown in **fig. 4**.

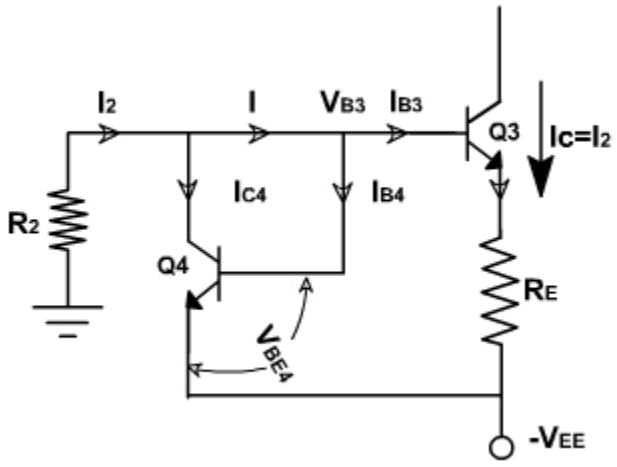


Fig. 4

Once the current I_2 is set up, the current I_{C3} is automatically established to be nearly equal to I_2. The current mirror is a special case of constant current bias and the current mirror bias requires of constant current bias and therefore can be used to set up currents in differential amplifier stages. The current mirror bias requires fewer components than constant current bias circuits.

Since Q3 and Q4 are identical transistors the current and voltage are approximately same

$$V_{BE3} = V_{BE4}$$

$$I_{B3} = I_{B4}$$

$$I_{C3} = I_{C4}$$

Summing currents at node V_{B3}

$$I_2 = I_{C4} + I$$

$$= I_{C4} + 2I_{B4} = I_{C3} + 2I_{B3}$$

$$= I_{C3} + 2\left(\frac{I_{C3}}{\beta_{dc}}\right)$$

$$= I_{C3}\left(1 + \frac{2}{\beta_{dc}}\right)$$

Generally β_{dc} is large enough, therefore $2/\beta_{dc}$ is small.

$$\therefore I_2 \approx I_{C3}$$

$$I_2 = \frac{V_{EE} + V_{BE3}}{R_2}$$

For satisfactory operation two identical transistors are necessary.

Example - 1

Design a zener constant current bias circuit as shown in **fig. 5** according to the following specifications.

(a). Emitter current $-I_E = 5$ mA

(b). Zener diode with $V_z = 4.7$ V and $I_z = 53$ mA.

(c). $\beta_{ac} = \beta_{dc} = 100$, $V_{BE} = 0.715$V

(d). Supply voltage - $V_{EE} = -9$ V.

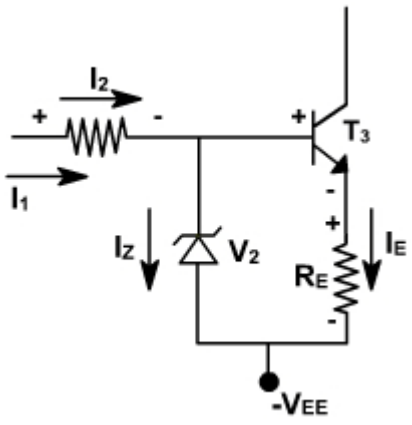


Fig. 5

Solution:

From **fig. 6** using KVL we get

$$V_{BE3} + I_{E3} R_E = V_z$$

$$\therefore R_E = \frac{V_z - V_{BE3}}{I_{E3}} = \frac{4.7 - 0.715}{5}\ k\Omega$$

$$= 0.757 k\Omega = 757$$

Practically we use $R_E = 820\ k\Omega$

Again $\quad I_2 = 1.2 I_{z1} = 1.2 \times 53 = 63.6 mA$

Again $\quad I_2 R_2 = V_{EE} - V_z$

$$\therefore R^2 = \frac{V_{EE} - V_z}{I_2}$$

$$= \frac{9 - 4.7}{63.6} \times 10^3\ \Omega = 67.6\Omega$$

Practically we use $R_2 = 68\ \Omega$

The designed component values are:

$R_E = 860\ \Omega$

$R_2 = 68\ \Omega$

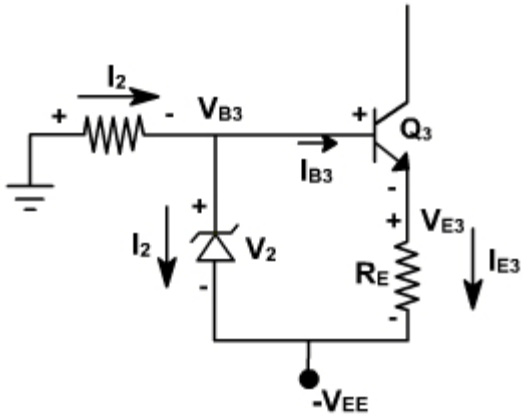


Fig. 6

Example - 2

Design the dual-input balanced output differential amplifier using the diode constant current bias to meet the following specifications.

1. supply voltage = ± 12 V.
2. Emitter current I_E in each differential amplifier transistor = 1.5 mA.
3. Voltage gain ≤ 60.

Solution:

The voltage at the base of transistor Q_3 is

$$V_{B3} = -V_{EE} + 2V_D$$
$$\therefore V_{E3} = V_{B3} - V_{BE3}$$
$$= -V_{EE} + 2V_D - V_{BE3}$$
$$\therefore I_{E3} = \frac{V_{E3} - (-V_{EE})}{R_E} = \frac{2V_D - V_{BE3}}{R_E}$$

Assuming that the transistor Q_3 has the same characteristics as diode D_1 and D_2 that is $V_D = V_{BE3}$, then

$$I_{E3} = \frac{V_D}{R_E}$$
$$\therefore R_E = \frac{V_D}{I_{E3}} = \frac{0.7}{1.5x2} x10^3 \qquad (I_{E3} = 2 \times 1.5 = 3mA)$$
$$= 233\Omega$$

Practically we take $R_E = 240\ \Omega$.

$$\text{Again} \quad R_2 = \frac{V_{EE} - 1.4}{1.5 \times 2} \times 10^3\ \Omega$$
$$= \frac{12 - 1.4}{1.5 \times 2} \times 10^3\ \Omega$$
$$= 3533\ \Omega = 3.533\ k\Omega$$

Practically we take $R_2 = 3.6\ k\Omega$.

$$I_{E3} = I_{E2} = 1.5mA$$
$$\therefore \quad r_e = \frac{25mV}{1.5mA} = 16.67\Omega$$

To obtain the differential gain of 60, the required value of the collector resistor is

$$R_C = A_d.r_e = 60 \times 16.67 = 1000.2\Omega$$
$$= 1\ k\Omega$$

The following **fig. 7** shows the dual input, balanced output differential amplifier with the designed component values as $R_C = 1K$, $R_E = 240\ \Omega$, and $R_2 = 3.6K\Omega$.

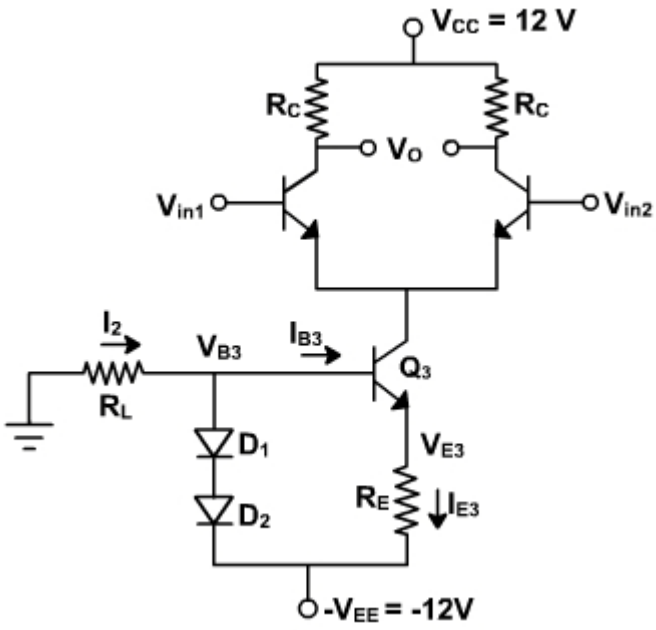


Fig. 7