*Name* : .....

*Roll No.* : .....

*Invigilator's Signature* : .....

**CS/BCA/SEM-1/BCA-101/2009-10**

**2009**

# DIGITAL ELECTRONICS

*Time Allotted* : 3 Hours | Full Marks : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

## GROUP – A
## ( Multiple Choice Type Questions )

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) A 3-bit synchronous counter uses flip-flops with propagation delay time of 20 ns each. The maximum possible time required for change of state will be

   a) 60 ns b) 40 ns

   c) 20 ns d) none of these.

   ii) BCD sutraction is performed by using which complement representation ?

   a) 1's b) 2's

   c) 10's d) 9's.

   iii) The SOP form of logical expression is most suitable for designing logic circuits using only

   a) XOR gates b) NOR gates

   c) NAND gates d) OR gates.

iv) The dual of a Boolean function is obtained by

a) interchanging all 0s and 1s only

b) changing 0s to 1s only

c) changing 1s to 0s only

d) interchanging all 0s and 1s and '+' and '.' signs.

v) When representing in the following code the consecutive decimal numbers differ only in one bit

a) Excess-3 b) Gray

c) BCD d) Hexadecimal.

vi) In a $J-K$ flip-flop when $J = 1$ and $K = 1$ and clock = 1 the output will be

a) toggle

b) 1

c) 0

d) recalls previous output.

vii) $(AB + A'B + A'B)$ is equal to

a) $A + B'$ b) $A' + B$

c) $A + B$ d) 1.

viii) 2's complement of 1010101 is

a) 0101011 b) 10101010

c) 1100000 d) 1000001.

ix) The basic fuse technologies used in PROM are

a) metal links b) silicon links

c) $p$-$n$ junctions d) all of these.

x) In general, a boolean expression of $(n + 1)$ variable can be implemented using a multiplexer with

a) $2^{n+1}$ inputs b) $2^{n-1}$ inputs

c) $2^{n}$ inputs d) None of these.

## GROUP – B

### ( Short Answer Type Questions )

Answer any *three* of the following. $3 \times 5 = 15$

2. Draw the neat diagram of 3-bits Bi-directional Shift Register using mode control ( $M$ ). When $M$ is logic zero then left shift and right shift for $M$ is logic one.

3. Design 2-bit Gray-Binary converter using basic logic gates with proper truth table.

4. Draw the logic diagram and truth table of $J$ - $K$ $f/f$. Why is $J$ - $K$ $F/F$ much more versatile that S - $R$ $F/F$ ?

5. What is a full subtractor ? Explain its basic structure with proper logic diagrams & truth tables. 1 + 4

6. Realize the funciton $f(A, B, C) = \Sigma\, m\,(1, 3, 5, 6)$ by a multiplexer. Discuss the operation logic.

## GROUP – C

### ( Long Answer Type Questions )

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Using $K$-map method minimize the following expression :

   $F(w, x, y, z) = m\Sigma\,(1, 5, 6, 12, 13, 14) + d\Sigma\,(2, 4)$.

   8

   b) Implement Ex-OR gate using NAND Gate and NAND gate using NOR gate. $3\frac{1}{2} + 3\frac{1}{2}$

8. a) Design and implement Mod-6 synchronous counter considering lock out problem. Is the counter self-starting ? 8 + 1

   b) Explain the difference between Ring and Johnson Counter with proper state diagram and circuit diagram.

   6

9. a) Explain the concept of parity checking.

   b) Discuss about the design of an odd parity generator.

   c) What is biased exponent in relation to Floating Point Representation ( FPR ) ?

   d) Represent ( – 1101011 ) in Floating Point Representation ( FPR ) for a 32-bit CPU. 3 + 4 + 3 + 5

10. What do you mean by race condition in flip-flop ? Design a *J - K* flip-flop and discuss its operation. Design and explain the functioning of the 4-bit adder-subtractor circuit.

    3 + 5 + 7

11. Write short notes on any *three* of the following : 3 × 5

    a) Universal gates

    b) Decoder

    c) Shift Register

    d) Flip-flop excitation table

    e) Ripple counter.